Manuel for sev seg disp: ~~https://digilent.com/reference/programmable-logic/basys-3/reference-manual?redirect=1~~

~~src1:~~ [~~https://www.chipverify.com/verilog/verilog-if-else-if~~](https://www.chipverify.com/verilog/verilog-if-else-if)

~~Src2:~~ [~~https://classes.soe.ucsc.edu/cse100/Spring22/lab/hierarchy/hierarchy.html~~](https://classes.soe.ucsc.edu/cse100/Spring22/lab/hierarchy/hierarchy.html)

~~Src3:~~ [~~https://inst.eecs.berkeley.edu/~cs150/Documents/Nets.pdf~~](https://inst.eecs.berkeley.edu/~cs150/Documents/Nets.pdf)

**How to use a test bench:** https://classes.soe.ucsc.edu/cse100/Spring22/lab/simulate/ug900-vivado-logic-simulation-minimized.pdf